REMARKS

By this amendment, independent claims 1, 3, 5, and 7 are amended and claims 13 and 14 are added to place this application in condition for allowance. Currently, claims 1-14 are before the Examiner for consideration on their merits.

In review, the Examiner has made two rejections of the claims, each one alleging that the claims are anticipated by either United States Patent No. 6,413,310 to Tamatsuka et al. or WO 00/12786. Since the published PCT application is the same as the Tamatsuka et al. patent, only Tamatsuka et al. (Tamatsuka) will be addressed in the arguments below. The rejections are addressed below by headings dealing with the invention, the applied prior art, and the arguments.

INVENTION

The invention is a solution to the problem of defects present on wafer surfaces. In the prior art, a number of techniques have been proposed to reduce the defects present on the surface of a wafer. In one mode, the speed of the pull of the single crystal ingot is retarded to produce zones that are COP free. While the defects are reduced in this technique, productivity is compromised, and this is not a practical solution to the problem.

Another technique is the doping of the single crystal silicon. This method has improved the quality of the wafers, but repeated cleanings of the wafers or subsequent processing still tends to introduce defects that compromise quality. Cleaning the wafers is particularly troublesome, since a wafer with undetectable defects may be transformed

into a subpar wafer as a result of the etching action of the cleaning step on these previously undetectable defects.

The present invention is a solution to the problem of unacceptable levels of defects, and particularly those defects present on wafers that are sliced or sliced and cleaned. By following the invention, a silicon single crystal wafer for a particle monitor is produced, which has extremely small surface density of light point defects (LPDs) on the wafer surface. This characteristic is accomplished by controlling the pulling of the silicon single crystal ingot from molten silicon material. More particularly, a time period of the single crystal passing a predetermined temperature range is closely controlled. This control is defined in claims 5 and 7 whereby the time period when passing through the temperature range of 1150 °C to 1070 °C is within 20 minutes and the time period passing through the temperature range of 900 °C to 800 °C is within 40 minutes. With this control, low COPs are attained on the whole region and to the whole depth of the thus obtained wafer.

Example 1 of the specification demonstrates that control of the defects as specified in the independent claims is achieved in the sliced or sliced and cleaned state regardless of the nitrogen content and in spite of six cleanings.

Example 2 shows the criticality of the control of the times at the specified temperatures. Referring specifically to Table 1, the comparative examples 2-1 to 2-4 show much higher count values. In addition, the treated wafers using the inventive processing, i.e., examples 2-5 to 2-7, also show improved BMD density as compared to the comparative examples 2-1 to 2-4. These demonstrations reveal, quite

unexpectedly, that after repeated cleanings, the defect is not increased beyond an unacceptable level.

In order to emphasize the nature of the invention, each of the independent claims is revised to define a sliced surface or a sliced and cleaned surface. As detailed below, the wafer of the invention is not the same as nor an obvious variant of the prior art and is deserving of patent protection.

TAMATSUKA

In the rejection, the Examiner alleges that Tamatsuka anticipates claims 1-12 on the grounds that:

1) a wafer is disclosed having a density of COP's with a size of 0.09 microns or more is 1.3 COPs/cm^2 or less;

2) a nitrogen content of 1×10^{10} to 5×10^{15} atoms/cm^2;

3) an oxygen concentration that is 18 ppm or less; and

4) the recited process limitations do not alter the fact that Tamatsuka discloses a wafer having the claim limitations.

In review, Tamatsuka relates to a production method wherein a single crystal ingot is grown by the CZ method and sliced into wafers. The wafer is then subjected to heat treatment under a non-oxidative atmosphere and then to a second heat treatment under an oxidative atmosphere without cooling to a temperature lower than 700 °C. This treated wafer is then used for a semiconductor device.

The initial heat treatment under the non-oxidative atmosphere conducted at 1100 °C to 1300 °C and the subsequent heat treatment under the oxidative atmosphere

without cooling the wafer to a temperature below 700 °C results in oxygen diffusing outwardly. The object of this two step heat treatment is to form a surface layer with low COPs. However, when repetitive cleaning is performed on the wafer surface, the surface layer containing the low level of COPs is removed by the etching action of the cleaning step, thus causing an abrupt increase in the density of LPDs.

ARGUMENT

Surface Density Limitation

To review, each of claims 1, 3, 5, and 7 define a surface density limitation on the wafer surface in light of repeated cleanings. Claims 13 and 14 are added to clarify that it is the sliced or sliced and cleaned surface of the wafer that contains the claimed density of particles.

In the rejection, the Examiner takes the position that the wafer of Tamatsuka is identical to that claimed, and therefore rejects the claims under 35 U.S.C. § 102(b).

In light of the amendments made above to claims 1 and 3 and the addition of new claims 13 and 14, each dependent on claims 5, and 7, respectively, it is respectfully contended that Tamatsuka cannot establish a *prima facie* case of anticipation against claims 1, 3, 5, and 7.

Each of claims 1, 3, 13, and 14 defines the wafer surface in two ways. A first way, based on the claim amendments or claim additions, wherein a sliced or sliced and cleaned wafer surface of the thus-formed ingot is defined. A second way defines that the surface density of particles having a particle size of not less than 0.12 μm on the sliced or sliced and cleaned wafer surface is not more than 15 counts/cm^2, even after

repeating a Standard Cleaning -1, which is made using alkaline chemical liquid mainly containing NH_4OH, H_2O_2, and H_2O.

Claim 1, for example, defines the invention in terms of the density of the sliced or sliced and cleaned surface. Claim 3 combines the density limitation with a nitrogen doping and the sliced or sliced/cleaned surface. Claim 13 combines the density limitation with the process control aspect of the invention and slicing or slicing and cleaning, and claim 14 combines the features of claims 1, 3, and 5 in combination with the sliced surface or the sliced and cleaned surface.

In Tamatsuka, the surface that the Examiner relies on to reject the claims is one that has been first formed by slicing and then by a two step heat treatment. However, Tamatsuka does not teach or suggest having a density of COP's meeting the claim limitation on the wafer surface after it has been sliced or sliced and repeatedly cleaned. In fact, there is no recognition of the density of the sliced surface of Tamatsuka, and the failure to teach this claim limitation means that Tamatsuka cannot anticipate claim 1 or claims 3, 13, and 14.

As described above, Applicants have discovered that a surface wafer that has a density less than 15 counts/cm^2 of particles not less than 0.12 microns is attained by control of the pulling process. This is confirmed by the test work described in Examples 1 and 2 of the specification. This discovery has not been made by Tamatsuka, nor can the Tamatsuka wafer meet the claim limitations regarding density for a sliced or sliced and cleaned ingot. Again, Tamatsuka goes about solving the problem of unwanted particles on the surface of the wafer in an entirely different manner, and the sliced or sliced and cleaned wafer of Tamatsuka cannot be considered to have the claimed level of density.

Since there is no basis to make this conclusion based on the teachings of Tamatsuka, any such allegation can only be the hindsight reconstruction of the prior art in light of Applicants' disclosure.

The Examiner also cannot allege that the defect density would be inherent in Tamatsuka. Table 1 of the specification shows that in order to meet the claimed density limitation, the time at temperature of the pulled ingot must be controlled. Without this control, the density count falls outside the claimed range.

For the reasons given above, Tamatsuka cannot be considered to teach each and every limitation of claims 1, 3, 13, and 14, particularly with regard to a sliced wafer surface or a sliced and cleaned wafer surface having the claimed density.

Lacking a basis to conclude that Tamatsuka anticipates the claims, the Examiner is left with relying on 35 U.S.C. § 103(a) to reject claims 1, 3, 13, and 14. However, there is no factual or objective basis to conclude that these claims are obvious in light of the teachings of Tamatsuka. As noted above, Tamatsuka is directed to a different mechanism to reduce the particle density on a given wafer. With a thrust in a direction entirely different from Applicants' aim, one of skill in the art would not or could not arrive at the instant invention based solely on the teachings of Tamatsuka. Thus, any rejection based on 35 U.S.C. § 103(a) would be improper and could not be sustained on appeal.

Process Control Limitations

It is further submitted that claims 5 and 7 are separately patentable over the applied prior art. In the rejection, the Examiner takes the position that the process limitations will not be given weight unless it is shown that they produce a materially different product. It is contended that the showing in the specification demonstrates that the process limitations

do produce a different product. That is, the sliced single crystal surface has a different surface if the pulling of the ingot is done according to the limitations found in the claims. Table 1 of the specification clearly shows this result and therefore, the wafer as defined in claims 5 and 7 is not the same as the wafer of Tamatsuka, which is totally silent regarding control of the pulling in the manner claimed. Consequently, the process limitations of claims 5 and 7 result in a sliced wafer with density characteristics that is materially different than the sliced wafer of Tamatsuka, and the rejection of claims 5 and 7 under 35 U.S.C. § 102(b) is flawed and should be withdrawn.

As with the claims 1, 3, 13, and 14, there is no basis to conclude that claims 5 and 7 are obvious over the teachings of Tamatsuka, especially when Tamatsuka is totally silent regarding affecting particle density on the wafer surface via control of the pulling rate in terms of time and temperature. Any allegation that Tamatsuka establishes a *prima facie* case of obviousness is pure hindsight, and such a rejection could not be sustained on appeal.

Dependent Claims

The remaining dependent claims 2, 4, 6, and 8-12 are patentably distinct over Tamatsuka by reason of their dependency on one of the allowable claims discussed above.

SUMMARY

It is respectfully submitted that by the amendments to claims 1 and 3 and submission of these changes as new dependent claims 13 and 14, each of claims 1, 3, 13, and 14 are patentably distinct over Tamatsuka. The grounds of patentability are

that Tamatsuka does not teach or suggest a sliced or sliced and cleaned wafer having the claimed density limitation.

Claims 5 and 7 are also patentable over Tamatsuka on the grounds that the process limitations found in the claims and the comparative evidence set forth in Table 1 of the specification show that using the claimed process limitations results in a materially different product, i.e., one not taught or suggest by Tamatsuka.

Accordingly, the Examiner is respectfully requested to examine this application in light of this amendment, and promptly pass claims 1-14 onto issuance.

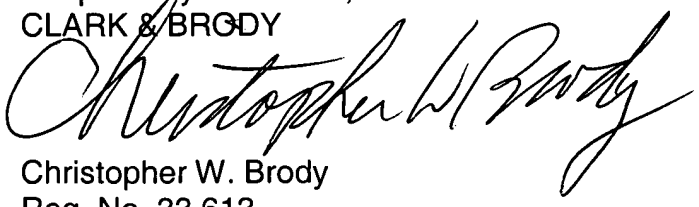
If the Examiner believes that an interview with Applicants' attorney would help expedite prosecution of this application, the Examiner is invited to telephone the undersigned at 202-835-1753.

The above constitutes a complete response to all issues raised in the outstanding Office Action of September 30, 2004.

Again, reconsideration and allowance of this application is respectfully requested.

Please charge any fee deficiency or credit any overpayment to Deposit Account No. 50-1088.

Respectfully submitted,
CLARK & BRODY



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